REMARKS

Applicant requests reconsideration and withdrawal of the rejections set forth in the above-mentioned Office Action, in view of the foregoing amendments and the following remarks.

Claims 1, 3-6, and 8-18 remain pending in this application, with Claim 1 being the sole independent claim. By this Amendment, Applicant amends Claims 1, 13, and 14. No new matter has been added.

Claims 1, 3, 6, 8-12 and 18 stand been rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,191,219 (Linke). Claims 4 and 5 stand been rejected under 35 U.S.C. § 103 as being unpatentable over the patent to Linke in view of U.S. Patent Publication No. US 2004/0042705 (Uchida, et al.). Applicant traverses these rejections for the following reasons.

Independent Claim 1 relates to an optical waveguide device comprising a slab-type optical waveguide layer, and a plurality of chips which include optical input and output ports for inputting and outputting an optical signal to and from the slab-type optical waveguide layer. An optical input port receives an optical signal, output by an optical output port, from the slab-type optical waveguide layer in accordance with a timing control signal inputted using an electrical connection between the plurality of chips. The optical signal output by the optical output port comprises a packet signal train formed of a finite pulse train. The timing control signal is individually sent as an instruction signal used to select adoption or rejection of the packet signal train.

Claim 1 has been amended to recite that the timing control signal comprises an electrical signal formed for every packet signal train.

By using a timing control signal comprising an electrical signal formed for every packet signal train, optical signals can be accurately received by chips even when the electrical signal of which the timing control signal is comprised is slower than the optical packet signal train to be transmitted.

In contrast, the patent to Linke is not understood to disclose or suggest a timing control signal comprising an electrical signal formed for every packet signal train of an optical signal output by an optical output port of a chip that inputs and outputs the optical signal to and from a slab-type optical waveguide, where the timing control signal is individually sent as an instruction signal used to select adoption or rejection of the packet signal train, as recited by amended Claim 1. Rather, this patent is understood to merely show that "broadcast information can be delivered selectively from transmitting subsystems to desired receiving subsystems either by including an address in the packet of optical pulses that alerts an addressed subsystem and energizes it to a receiving mode. Alternatively, a control system can be used to provide appropriate clock pulses to control electrically the appropriate synchronization of the transmitting and receiving modes of the various subsystems." (column 1, line 62 through column 2, line 2).

For this reason, amended independent Claim 1 is not anticipated by the Linke patent.

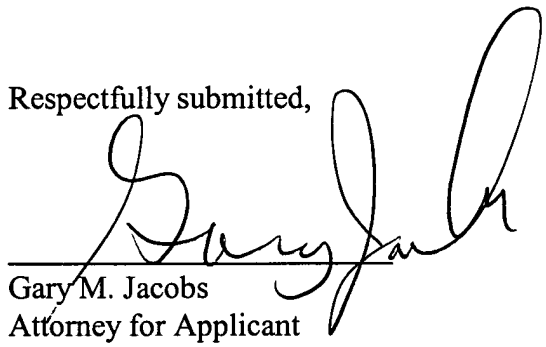
Applicant submits that the dependent claims are allowable, in their own right, for defining features of the present invention in addition to those recited above with respect to

independent Claim 1. Therefore, Applicant requests individual consideration of the dependent claims.

In view of the above amendments and remarks, the application is now in allowable form. Therefore, early passage to issue is respectfully solicited.

Applicant's undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our address given below.

Respectfully submitted,



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